

EN201 - Correction du TD n°2

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Question n°1 - Synthèse comportementale

```
ENTITY circuit IS
  PORT ( A, B, C, RESET, W : IN std_logic;
        H : IN std_logic;
        S1, S2 : OUT std_logic);
END circuit;

ARCHITECTURE Behavioral OF circuit IS

  SIGNAL S0 : std_logic;

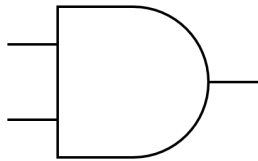
  BEGIN

    S1 <= S0 WHEN W ='1' ELSE A;

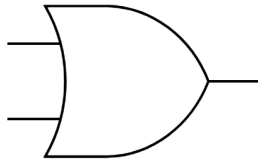
    PROCESS (RESET, H)
    BEGIN
      IF (RESET ='0') THEN
        S0<='0';
        S2<='1';
      ELSIF (H'event AND H='1') THEN
        S0<= NOT ((A AND B) OR C);
        S2<=A AND B AND C;
      END IF;
    END PROCESS;

  END Behavioral;
```

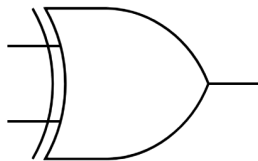
Question n°1 - Synthèse comportementale



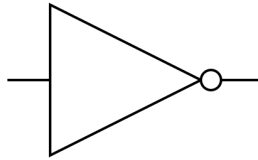
AND



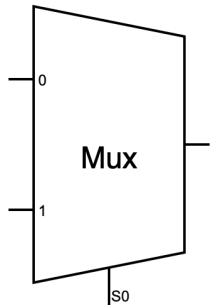
OR



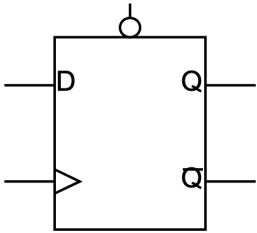
XOR



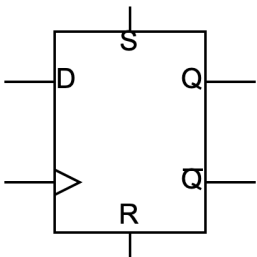
NOT



Multiplexeur 2:1

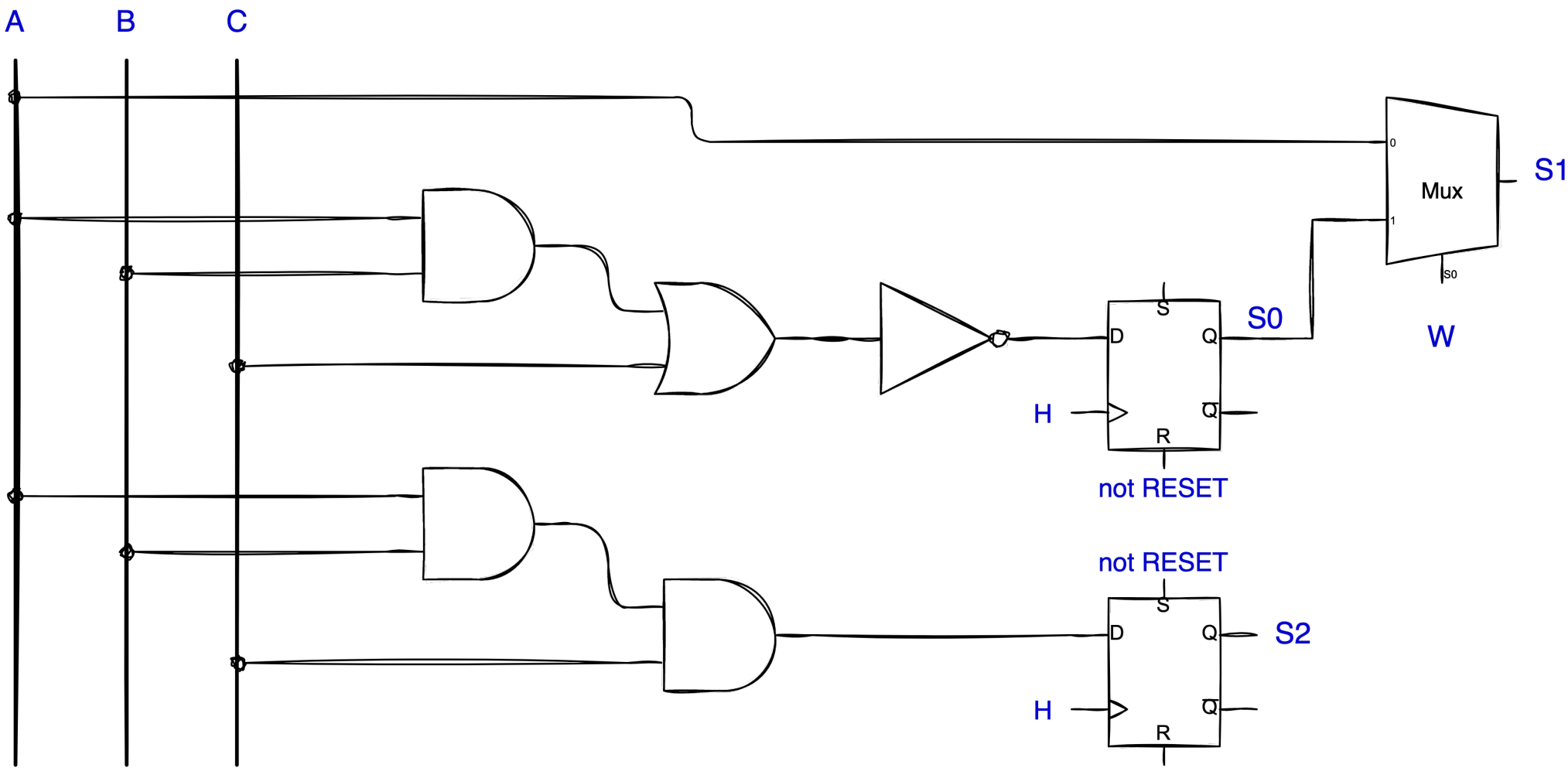


Bascule D avec reset asynch.

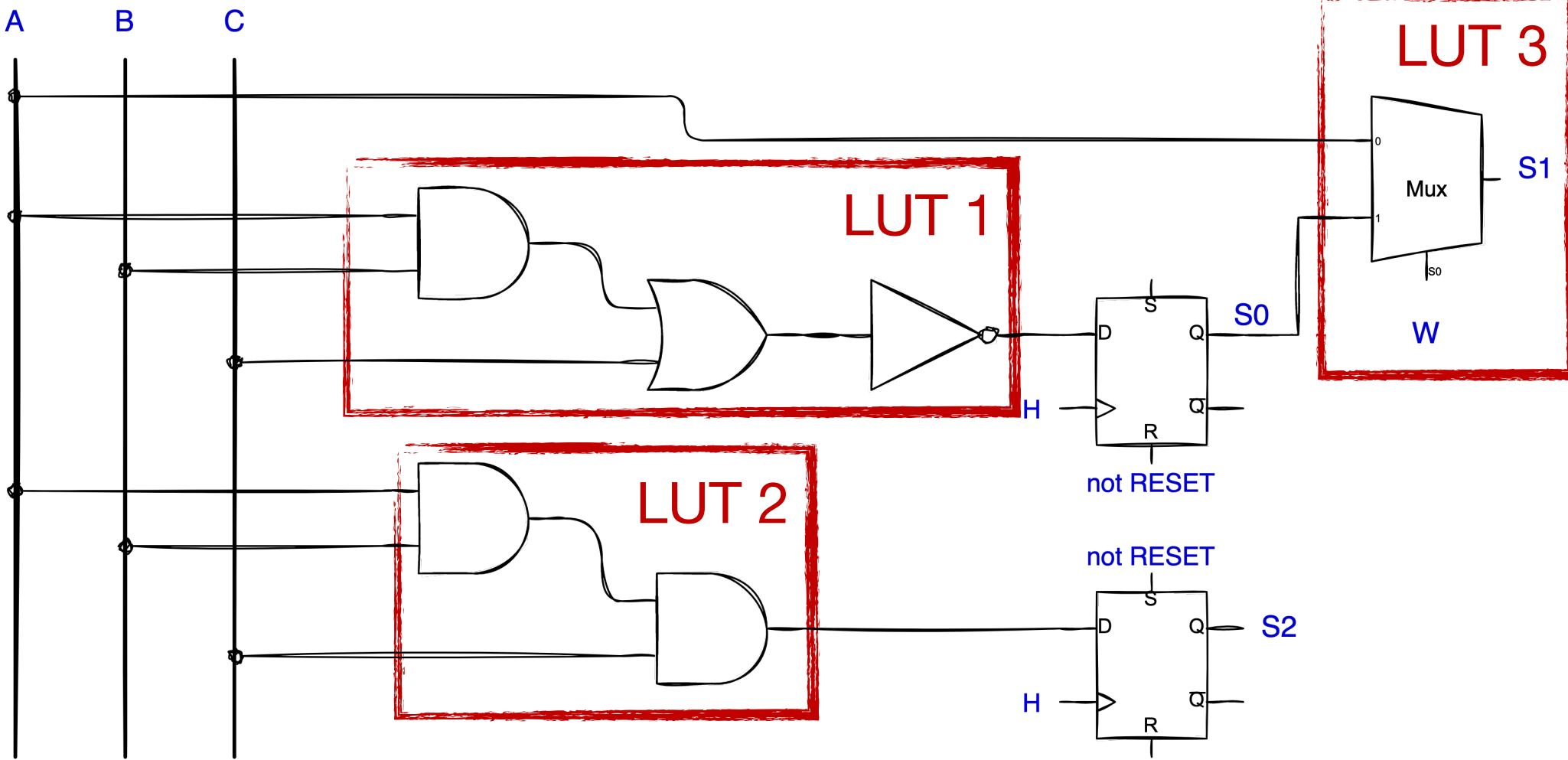


Bascule D avec set/reset synch.

Question n°1 - Synthèse comportementale



Question n°2 - Estimation du nombre de LUTs



Question n°2 - Tables de vérités des LUTs

LUT 1

A	B	C	S0
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

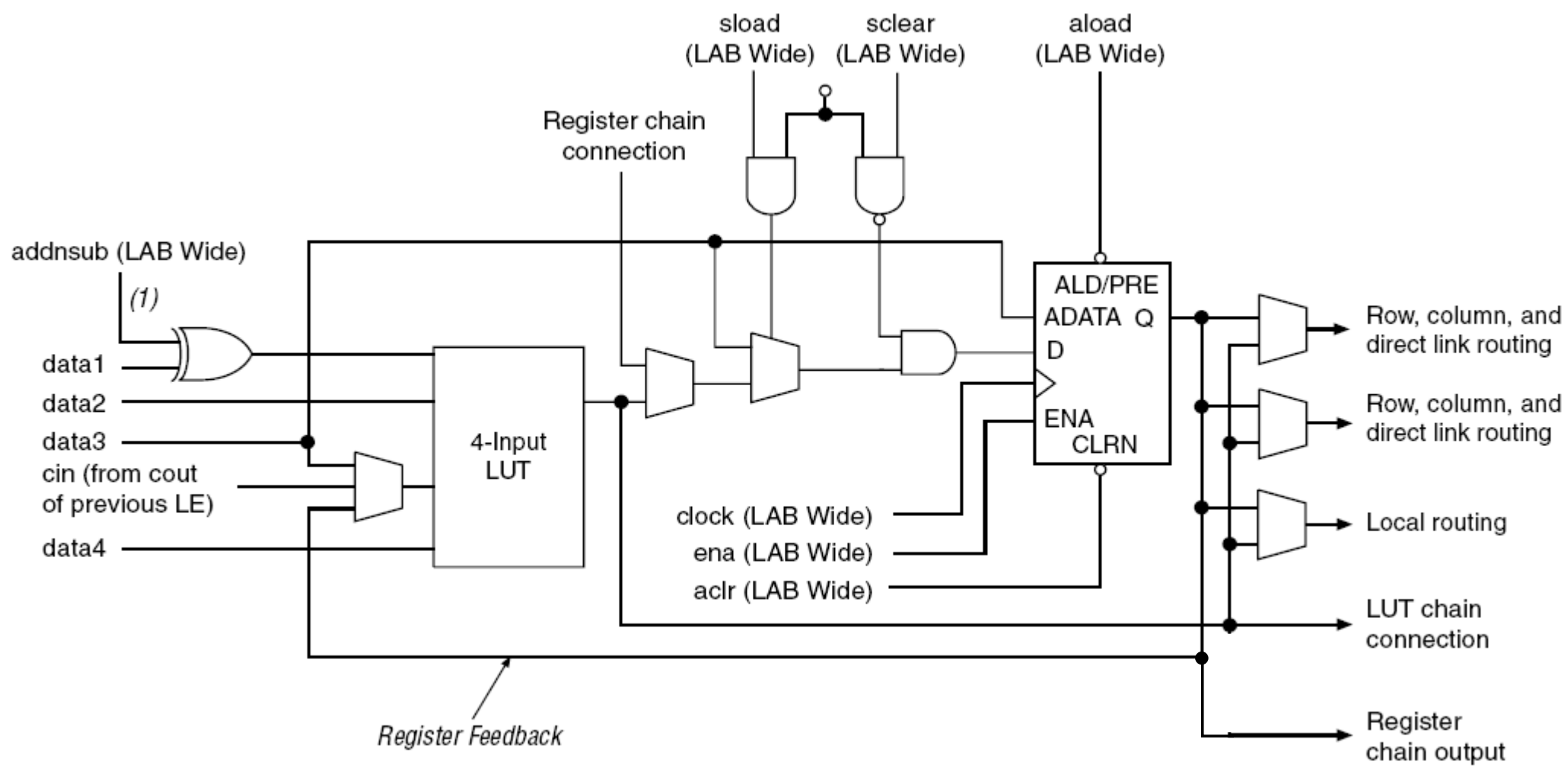
LUT 2

A	B	C	S2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

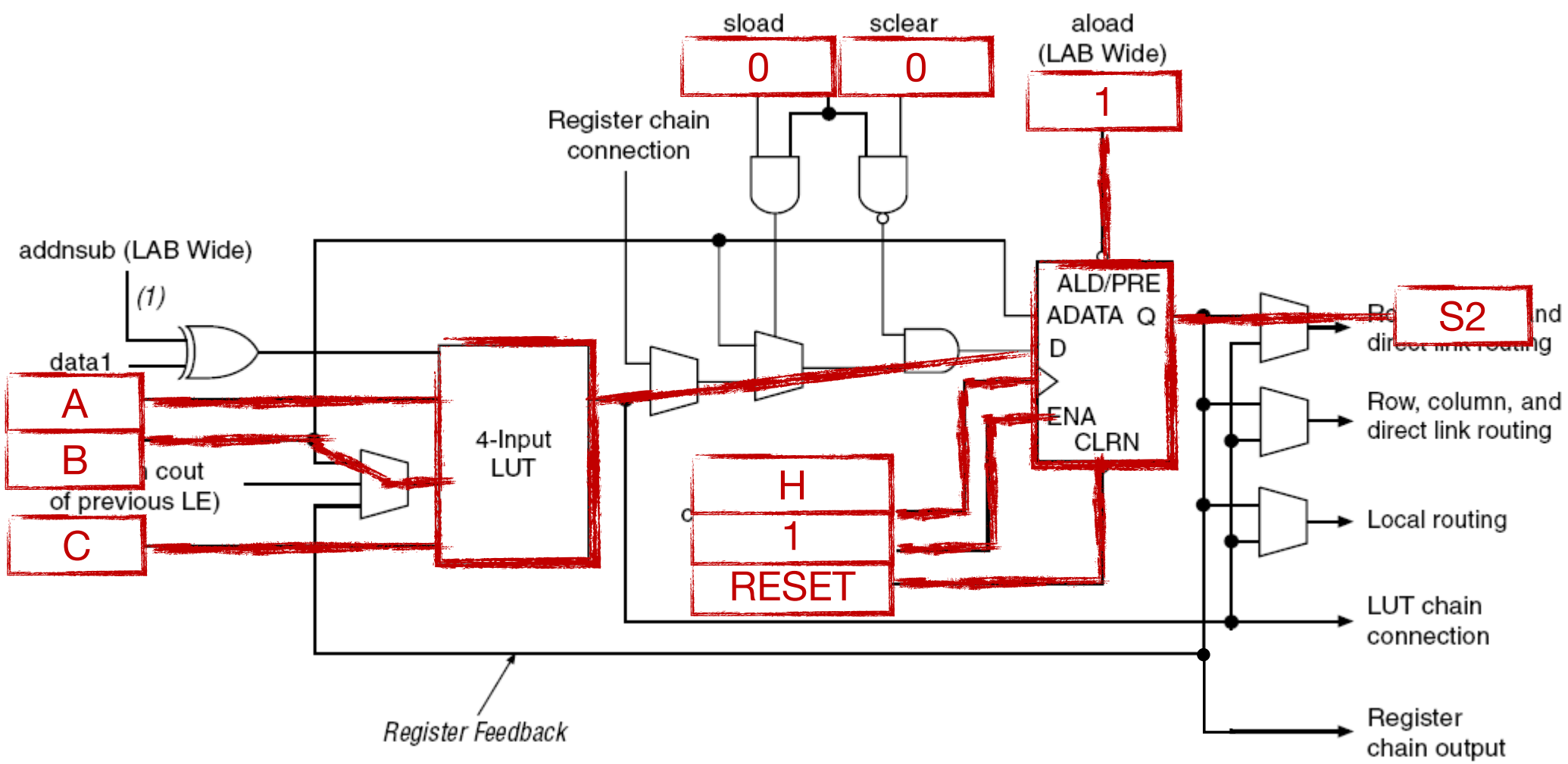
LUT 3

W	A	S0	S1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

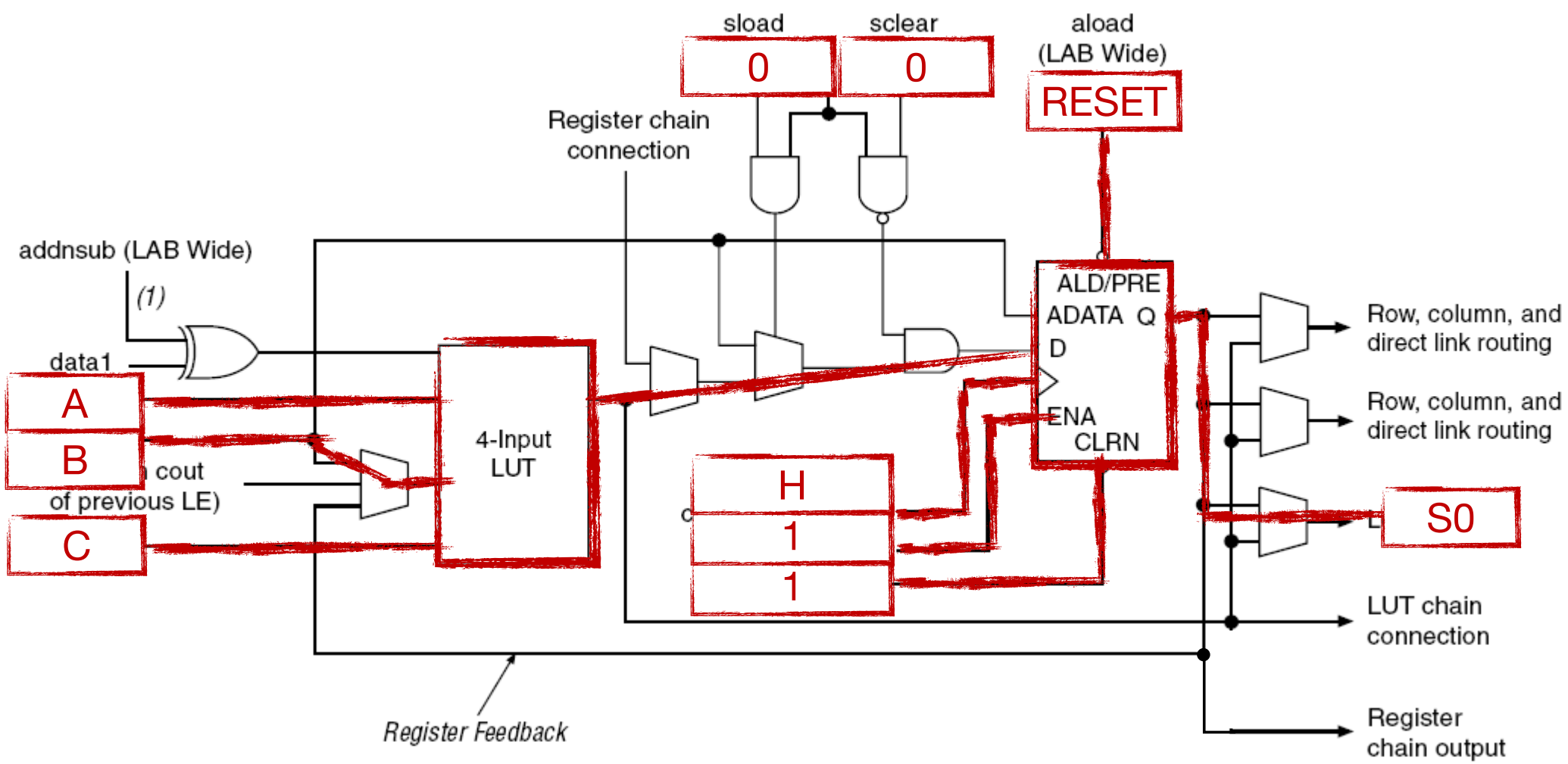
Question n°3 - Mapping technologique



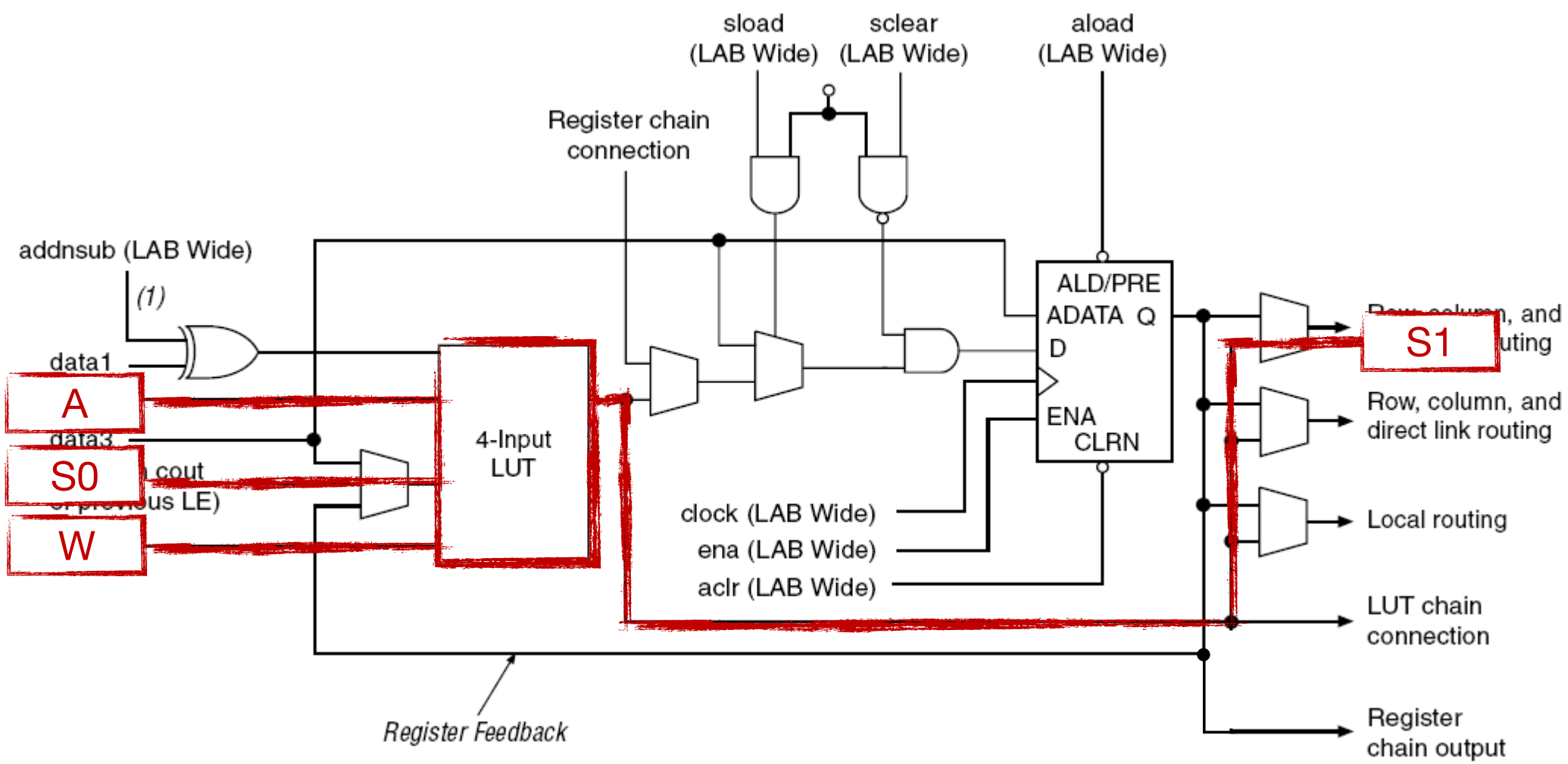
Question n°3 - Mapping technologique



Question n°3 - Mapping technologique



Question n°3 - Mapping technologique



Question n°4 - Placement des cellules et routage

